

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

1. (Canceled)
2. (Previously Presented) An insulated gate semiconductor device, comprising
  - a layered structure on an essentially planar cathode side of a semiconductor substrate, said layered structure being arranged around a cell window and forming an insulated gate comprising an oxide layer on top of said semiconductor substrate and a poly-silicon layer on top of said oxide layer,
  - a first doped region of a first conductivity type extending into the substrate beneath the centre of said cell window,
  - a second doped region of a first conductivity type, in particular a shallow base region, extending into the semiconductor substrate beneath the outer edge of the cell window adjacent said first doped region;
  - at least one third doped region of a second conductivity type, in particular a source region, extending partially into said second doped region adjacent said first doped region; and
  - a first main contact disposed on the top surface electrically connected to said first doped region and said third doped region;wherein

- at least two isolated strips are arranged in the cell window between the insulated gate and the first main contact, dividing the cell window in an outer cell window region and an inner cell window region, said outer cell window region being located between the isolated strips and insulated gate and above the third doped region, and said inner cell window region being located between the isolated strips and comprising the main contact, said strips comprising an oxide layer on top of the semiconductor substrate and a poly-silicon layer on top of the oxide layer, wherein
- the two strips comprise openings, and wherein
- the third doped region extends into the substrate beneath the openings, electrically connecting the third doped region beneath the outer cell window region to the first main contact.

3. (Previously Presented) An insulated gate semiconductor device as in claim 2, wherein

- the ratio length of openings to lengths of strips is laid out to match a desired emitter ballast resistance.